

FIGURE 1
(PRIOR ART)

10003643-110201

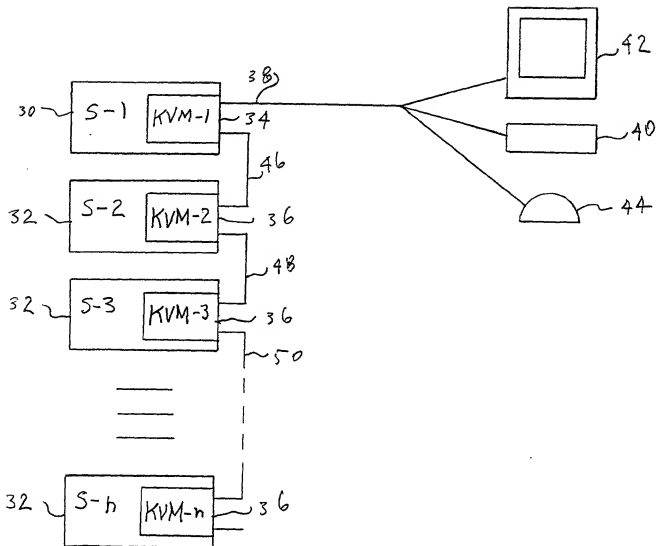


FIGURE 2
(PRIOR ART)

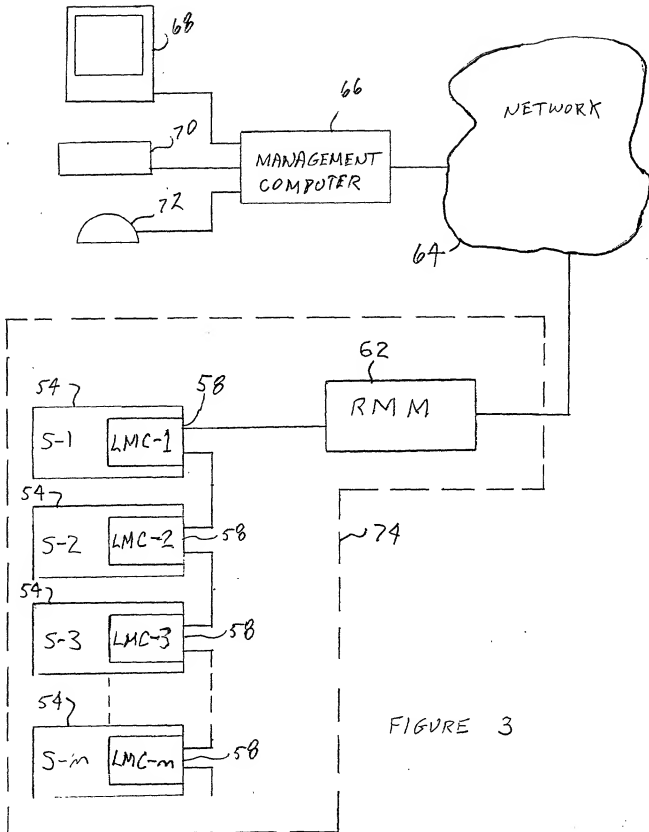
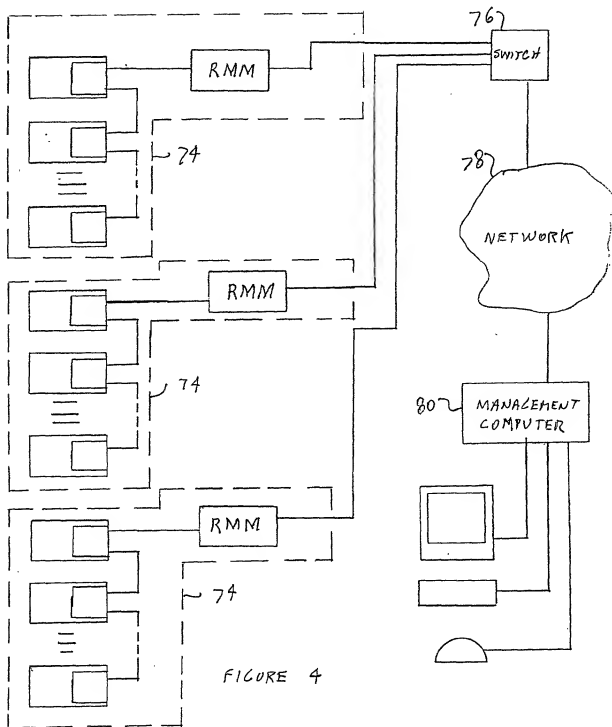


FIGURE 3

10003549-110201



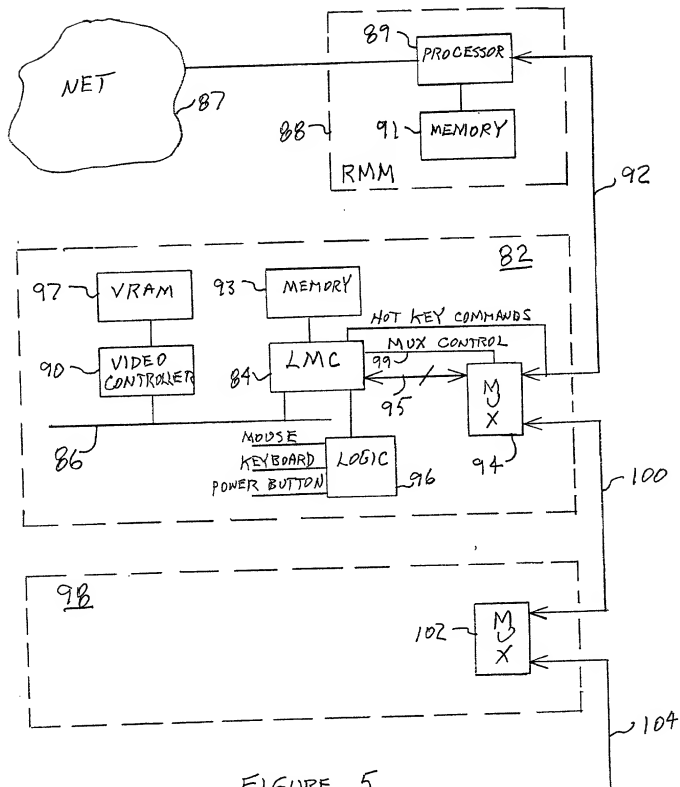


FIGURE 5

10003619.110201

The diagram illustrates a multi-processor system architecture. At the top, a dashed box labeled 104 contains an RMM (110) and an I²C MASTER (114). The RMM (110) is connected to a NET line (116) and a bus (124). The I²C MASTER (114) is connected to the bus (112) and the I²C SLAVE (118). The bus (124) connects to a MUX (122) and a MUX (128). The MUX (122) is connected to the I²C SLAVE (118) and the LMC LOGIC (106). The MUX (128) is connected to the I²C SLAVE (126) and the LMC LOGIC (108). The LMC LOGIC (106) and LMC LOGIC (108) are connected to the MUX (122) and MUX (128) via lines 136 and 137. The MUX (122) and MUX (128) are connected to the bus (130) via lines 132 and 134. The bus (130) connects to the I²C SLAVE (118) and the I²C SLAVE (126).

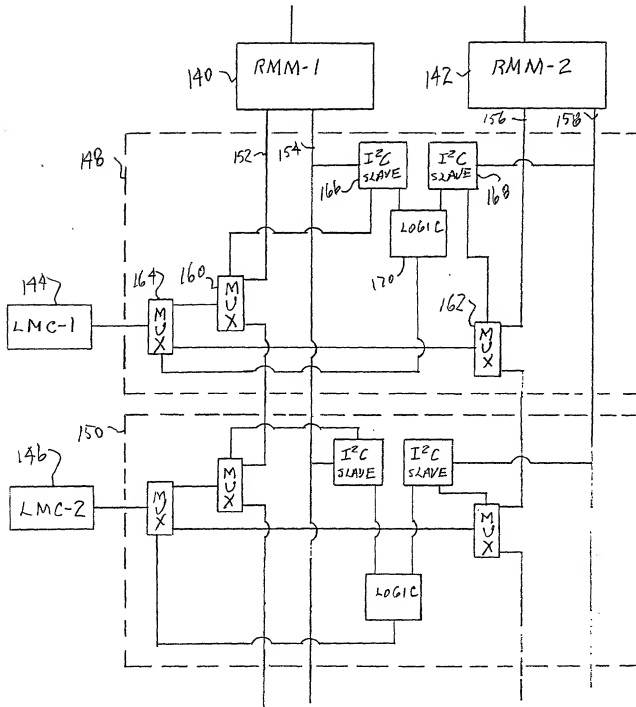


FIGURE 7

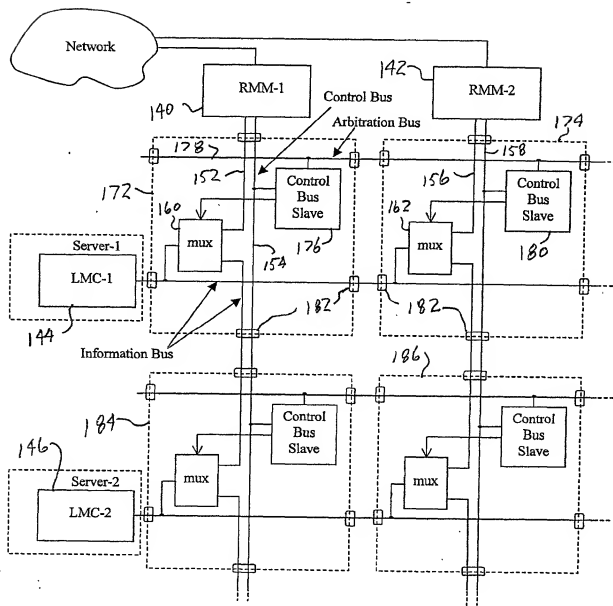


Figure 8

10003649.110201

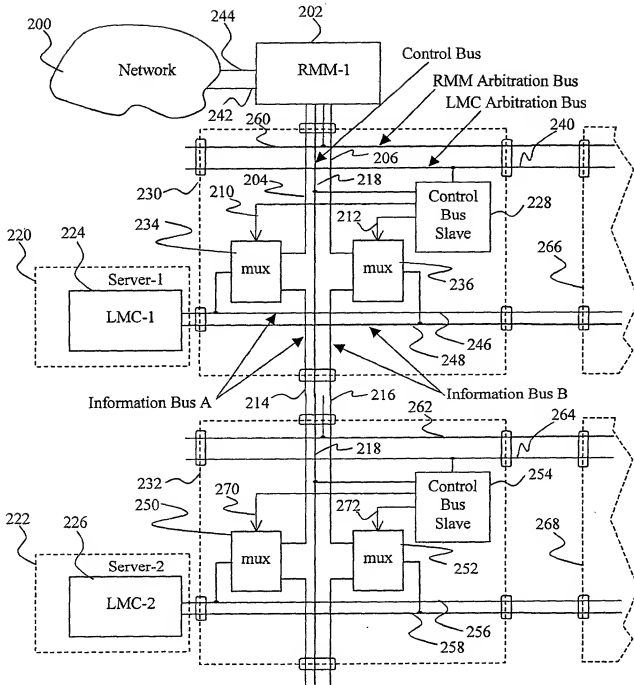


Figure 9